Integrated VCOs employing FBARs for direct oscillation of Rb clock frequency

Rb 時計周波数の直接発振を目的とした FBAR-VCO の開発

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1. Introduction

Timing synchronization based on the Global Navigation Satellite System (GNSS) is widely accepted in various smart systems like a real-time data-acquisition from an enormous number of devices. When putting the quasi-zenith satellites into service in Asia-Pacific area, the application fields of GNSS will be acceleratingly expanded. However, the stability of GNSS based synchronization heavily depends on the radio-wave-location. It is not sufficiently robust.

Here, an atomic clock was spotlighted as a back-up system of the GNSS receiver. If the atomic clock is miniaturized to the chip level which can be mounted on the wireless module board by a Flip Chip Bonding (FCB), the clock can keep the synchronization without frequent communication to the satellites. Commercial Chip Scale Atomic Clocks (CSACs), however, is not so small and low power consumption to integrate into the consumer devices or sensor nodes[4].

It is known that the radio frequency (RF) circuitry is a key to compress the size, cost and driving-power. In this study, a simple PLL-free RF circuit was proposed to lock the atomic clock frequency. By using a thin Film Bulk Acoustic Resonator (FBAR) for the frequency reference of a voltage controlled oscillator (VCO) instead of a bulky quartz resonator, the clock frequency can be directly outputted without any multiplication stages.

2. Design and Fabrication

Conventionally, a PLL circuitry must be integrated to assign the atomic resonance. In this study, to shrink the circuit scale and power consumption, the PLL-free system was discussed. By employing the 3.5-GHz band FBAR instead of the quartz resonator, the clock frequency (3.417 GHz) can be directly outputted from the simple oscillator without multiplier and PLL. Figure 1 shows a topology of designed circuit. A g_m-boosted differential oscillator was adopted, in which a cross coupling (CC) oscillator and a balanced Colpitts (CP) oscillator were parallelly combined[1]. This circuit has advantages of both CC and CP oscillators. A CC oscillator shows a good oscillation stability and low phase noise performance. Also, CP oscillator has a good durability for the parasitic capacitance.

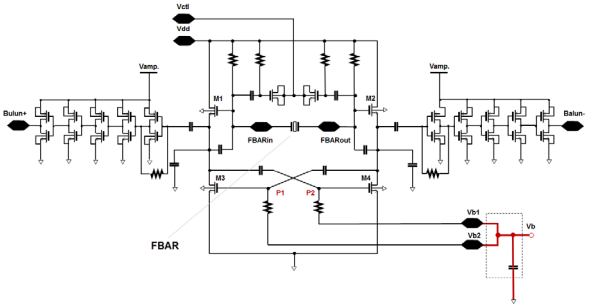

Figure 1. Topology of the FBAR-VCO

Table I. Typical characteristics of 3.5-GHz band FBARs

Capacitance C_0	k_{eff}^2
0.10 pF	4.6%
Resonant Freq. f_r	Resonant Q Q_{r_load}
3.4 GHz	1100
Anti-resonant Freq. f_a	Anti-resonant Q Q_{a_load}
3.5 GHz	730

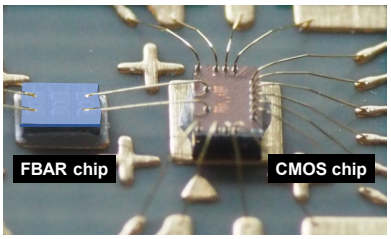

Figure 2. The FBAR-VCO on the evaluation board

The circuit shown in Fig. 1 was implemented in a 65-nm CMOS technology. The circuit die size was 1 mm × 0.67 mm. Typical values of characteristics of the 3.5-GHz band FBAR are summarized in Table I. Figure 2 shows a fabricated oscillator. The FBAR chip was connected to the circuit on the board by wire bonding technique.

3. Evaluation

Typical oscillation characteristics of the

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Table 2. comparison of state-of-art BAW oscillators.

	f_{osc} [GHz]	P_{dc} [mW]	Assembly	Technology	Resonator type	PN @1MHz	FoM @1MHz	App.
S. Razafimandimby et. al. [2]	2.15	12.0	FCB on IC	0.25 µm SiGe BiCMOS	SMR	-145	-201	General RF system
R. Boudot et. al. [3]	2.09	18.2	Wire bonding to IC	0.25 µm SiGe BiCMOS	SMR	-151	-205	General RF system
P. Guillot et. al. [4]	2.00	0.9	Wire bonding to IC	65 nm Si CMOS	SMR	-148	-214	General RF system
S. Romisch et. al.[5]	4.60	9.8	Discrete	-	SMR	-124	-187	Cs atomic clock
This work	3.40	9.0	Wire bonding to IC	65 nm Si CMOS	FBAR	-140	-201	Rb atomic clock

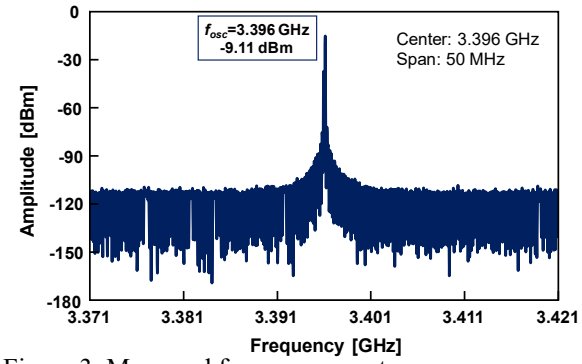

Figure 3. Measured frequency spectrum

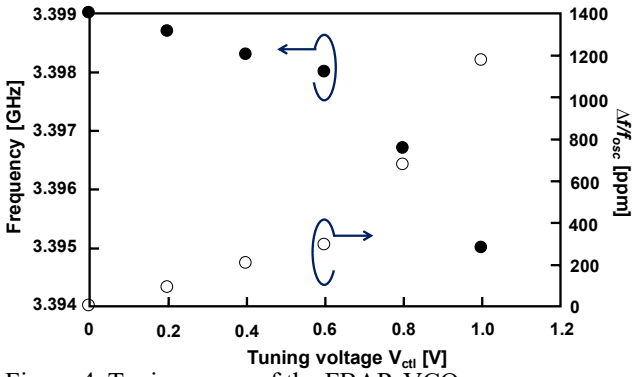

Figure 4. Tuning range of the FBAR-VCO

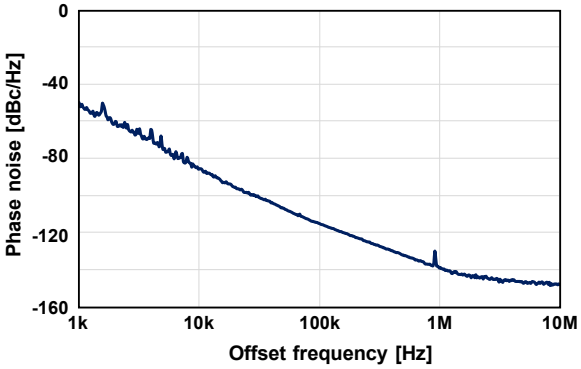

Figure 5. Measured phase noise performance

oscillator was shown in Fig. 3. V_{dd} and V_{ctl} were set to 1.0 V and 0 V, respectively. Consumed power was 9.0 mW. The oscillation frequency was 3.396 GHz. It was 21 MHz smaller than target clock frequency (3.417 GHz). A maximum tuning range was 4.5 MHz (1200 ppm) when the V_{ctl} was tuned within 0 to 1 V (Fig.4). Figure 5 shows a phase noise (PN) of the oscillators. The PN at 100 kHz and 1 MHz was -115 and -140 dBc/Hz, respectively.

Table 2 shows a comparison of state-of-art BAW (Bulk Acoustic Wave) oscillators. Figure of merit of the oscillator was defined as follows:

$$FoM_{osc} = L(f) - 20\log\left(\frac{f_{osc}}{f}\right) + 10\log\left(\frac{Pdc}{1\text{mW}}\right) \quad (1),$$

where $L(f)$, f_{osc}, and P_{dc} are phase noise at a given offset f, oscillation frequency and dc power, respectively.

4. Conclusion

We developed the voltage controlled oscillator for a Rb atomic clock. A balanced g_m-boosted type oscillator was adopted and was implemented by 65-nm CMOS process. By using a 3.5 GHz-band FBAR as a frequency reference instead of the bulky quartz resonator, a simple architecture without PLL circuitry and multiplier was achieved. As an evaluation result, the fabricated chip was oscillated at 3.40 GHz with a phase noise of 140 dBc/Hz on the offset frequency of 1 MHz. Power consumption was 9.0 mW. The tuning range was 1200 ppm.

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