

**Negative-resistance simulation in NMOS Colpitts crystal oscillators**  
NMOS コルピッツ水晶発振回路における負性抵抗算出法

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**1. Abstract**

Crystal oscillators have been widely used in wireless applications to provide a timing reference signal. It has recently become necessary to lower the power consumption and improve applications by designing low voltage driven oscillators [1].

Various methods for analyzing negative resistance have been proposed for Colpitts crystal oscillators that use BJT, CMOS and NMOS amplifiers[2-5].

A method for analyzing negative resistance for oscillators using NMOS (Negative-MOS) with its small signal level of negative resistance to steady the oscillation level is proposed in this paper. In particular, the gate current of NMOS has a lower power consumption that makes it almost negligible.

The input and output characteristics( $V_{GS} - I_D$  characteristic) of NMOS circuits are formulated from the cutoff, saturation and triode regions. It is difficult to calculate each region because the boundary condition included in the equation of each region is different. Thus, the approximation of the operating characteristics can be derived from making a polynomial approximation of the input and output characteristics calculated by using the DC characteristic. The mutual conductance ( $g_m$ ) and negative resistance can be calculated by numerically integrating the approximation.

**2. Structure of NMOS oscillators**

Figure 1 shows a Colpitts crystal oscillator with an NMOS of the modified equivalent model.

According to Fig. 1 the impedance  $Z_{in}$  can be derived and be represented using the following equation.

$$Z_{in} = R_G // Z_3 // (Z_1 + Z_2 + g_m \cdot Z_1 \cdot Z_2) // \frac{(Z_1 + Z_2 + g_m \cdot Z_1 \cdot Z_2) \cdot Z_3}{g_m \cdot Z_1 \cdot R_D} \quad (1)$$

**3. Derivation of  $g_m$**

The voltage between the gate and source  $V_{GS}(t)$  can be represented by using the following equation

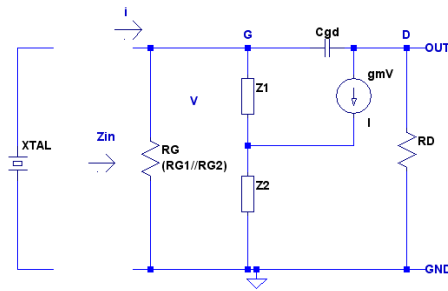


Fig. 1 Colpitts crystal oscillator with NMOS of modified high frequency equivalent model

$$V_{GS}(t) = V_{GS0} - Z_2 \Delta I_D + V_{GSW} \sin \omega t \quad (2)$$

$V_{GS0}$  is the voltage between the gate and source under a DC bias and  $\Delta I_D$  is the increment from the bias current  $I_{D0}$ .  $V_{GSW}$  is the amplitude of the AC voltage between the gate and source.

The input and output characteristics can be calculated by substituting  $V_{GS}(t)$  from 0 to  $V_{DD}$  for calculating  $I_D(t)$ . The result is derived from the polynomial of degree n, where n = 20, and then  $I_{D\_app}$  can be derived by using the polynomial approximation.

$$I_{D\_app}(V_{GS}) = a_0 + a_1 V_{GS} + a_2 V_{GS}^2 + a_3 V_{GS}^3 + \dots + a_{20} V_{GS}^{20} \quad (3)$$

Where,  $a_0, a_1, a_2, a_3, \dots, a_{20}$  are the coefficients

Based on Eq. (3), when the operating point is  $V_{GS}(t) = V_{GS0}$ , the current ( $I_{D0}$ ) will be derived using the following equation.

$$I_{D0} = I_{D\_app}(V_{GS0}) \quad (4)$$

The DC portion of the drain current  $I_{DC}$  and the fundamental frequency magnitude can be derived from Eq. (2) using a Fourier transform which are represented by using the following equations and the results can be calculated by using numerical integration

$$I_{dc} = \frac{1}{2\pi} \int_{-\pi}^{\pi} I_{D\_app}(V_{GS}(t)) d\omega t \quad (5)$$

$$I_w = \frac{1}{\pi} \int_{-\pi}^{\pi} I_{D\_app}(V_{GS}(t)) \sin \omega t d\omega t \quad (6)$$

$\Delta I_D$  can be derived from equation (4) and equation (4) and represent as below equation.

$$\Delta I_D = I_{dc} - I_{D0} \quad (7)$$

Substituting Eq. (5) for Eq. (2), and then perform a feedback,  $g_m$  can be represented by using the following equation.

$$gm = \frac{I_w}{V_{GSW}} \quad (8)$$

Here,  $g_m$  has been nonlinearly taken into account.  $Z_{in}$  can be calculated by substituting in this resulting  $g_m$  for Eq. (1). The real part of  $Z_{in}$  is the negative resistance.

#### 4. Simulation results

Figures 2 and 3 represent the  $I_C$  and  $I_D$  characteristics and calculated approximation results when the supplied voltage is 5V.

A ripple occurs when the polynomial approximation based on the current characteristic of a BJT is sharp. Therefore, the approximation result is separated from the theoretic value. In contrast, the MOS results were basically consistent.

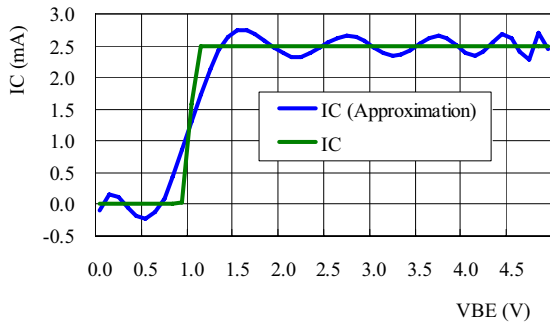


Fig. 2  $I_C - V_{BE}$  characteristics and approximation result of BJT

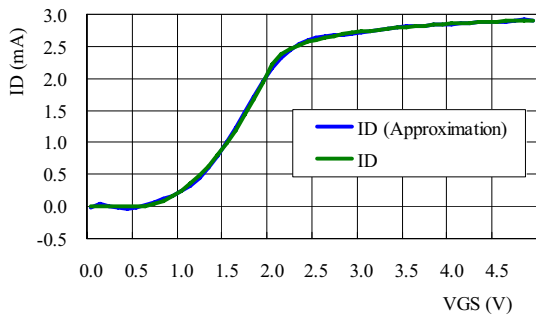


Fig. 3  $I_D - V_{GS}$  characteristics and approximation result of NMOS

$I_w$  can be derived by substituting this approximation for Eq. (6).  $g_m$  can be calculated from Eq. (8). The negative resistance can be derived from by substituting the calculated  $g_m$  for Eq. (2). The negative resistance of BJT is much larger because the  $g_m$  of the BJT and CMOS are different.

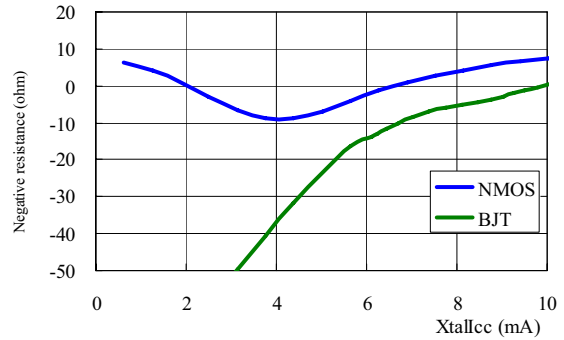


Fig. 4 Negative resistance characteristic of BJT and NMOS crystal oscillators

#### 5. Conclusion

We analyzed the negative resistance of BJT and NMOS circuitry. The input and output characteristics of NMOS using a polynomial approximation are basically consistent.

The negative resistance of NMOS is smaller because the  $g_m$  is smaller, but it is obvious that the negative resistance calculation is simplistic based on the simulation. Our future work will be to compare these simulation results and the actual measurements taken from a NMOS oscillator.

#### References

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