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On-wafer measurement of power durability for Surface Acoustic Wave Devices
弾性表面波デバイス用耐電力オンウェハ測定系の構築

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1. Introduction

Power durability (PD) is one of the most important properties for surface and bulk acoustic wave (SAW/BAW) devices.[1]. Their time to failure (TF) τ is dependent on not only the incident power P but also chip tempreture T and driving frequency f [2]. Excess P and/or T are often applied to shorten τ (accelaration test).

It is known[1-3]. that the relation among τ, P and T is expressed well by the following Eyring model[3]:

$$\tau = \alpha \times \exp\left[\frac{E}{(k \cdot T)}\right] \times P^{\beta} , \qquad (1)$$

where k and E are the Boltzmann constant and active energy. However, procedures to determine constants α and β in Eq. (1) have not been standardized, and thus each SAW/BAW company determined the dependency by its own way.

As a first step for the standarization, this paper reports construction of an on-wafer measurement system for PD of SAW/BAW devices. This setup allows us to set P and T independently.

By the way, it is not easy to monitor T when the device under test (DUT) is packaged. In Ref. [3], the temperature sensor was embedded on the SAW chip for this purpose. However this approach is somewhat impractical because special chip design and fabrication are required.

This paper also describes a simple technique for T monitoring. It employs the cut-off frequency f_B of BAW radiation as a temperature sensor. Theoretically, f_B is independent of the chip surface condition and parasitic impedanece.

2. Measurement System for Power Durability

Figure 1 shows the constructed measurement system. A sinusoidal signal generated by a signal generator (SG) is amplified by a power amplifier (PA), and is fed to DUT through a wafer probe. The DUT is placed on a temperature-controlled Cu stage.

Every 10 minutes during the PD test, the DUT

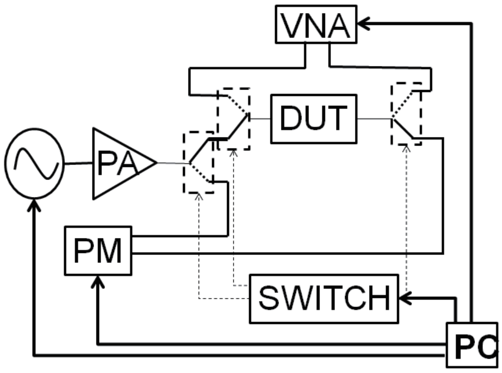

Fig. 1 Setup of the measurement system

condition is monitored by a vector network analyzer (VNA). Three switches (SWs) are used to switch the circuit to the monitor mode from PD test. All these instruments are controlled by a computer, which also logs VNA and PM outputs until failure of the DUT.

Losses in cables, SWs and wafer probes are measured in advance, and their influence is compensated at the PD test. The input and output power is monitored by a power meter (PM).

Ladder-type SAW filters fabricated by Taiyo Yuden were used as the DUT in the following experiments. It should be noted that conventional Al alloy is chosen as the electrode material in this stage so as to shorten τ.

Figure 2 shows an example of the result when f=1.98 GHz and P=1.2 W. Right after the power on, the filter insertion loss decreased rapidly. This may be due to desorption of moisture from the SAW propagation surface. After that, the passband shape and the insertion loss scarcely changed for a while, and the DUT was suddenly corrupted at 90 min.

Series of PD tests were performed, and relation between P and τ was investigated for the given SAW device structure.

Fig. 3 shows the result. It is seen that log(τ) changes linearly with log(P) as we expected from Eq. (1).

The least square fit for the data gives

$$\tau = 10^{4.8} \cdot P^{-13.9} . \qquad (2)$$

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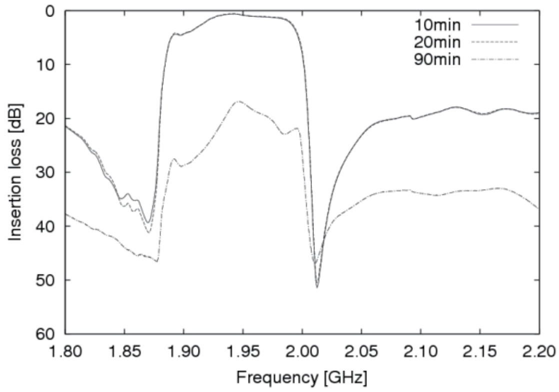
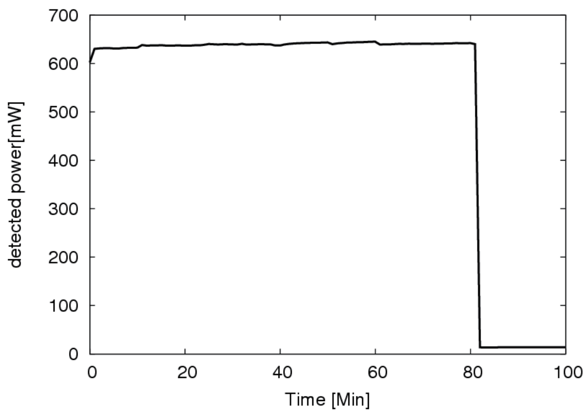


(a) Variation of frequency response



(b) Variation of output power

Fig. 2 Logged results when P=1.5 W.

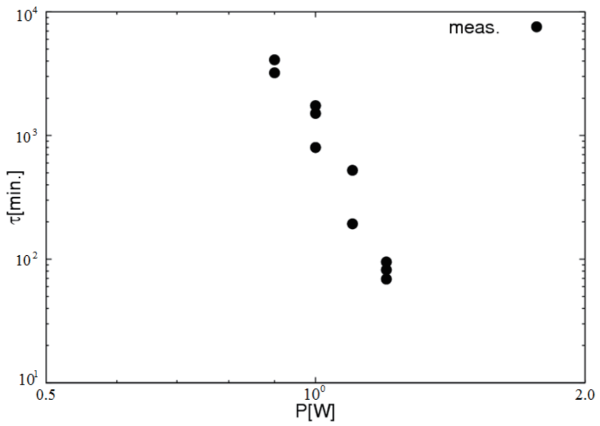


Fig.3 Relation between P [W] and τ [sec].

3. Estimation of Chip-Surface Temperature

SAW devices are designed so that f_{B} locates in the rejection band. Or they will cause excess insertion loss in the passband. Thus f_{B} can be found easily in the VNA output. For example, f_{B} can be seen at 2.09 GHz, where the insertion loss changes irregularly with frequency. At least two f_{B} exist in the ladder filter response. Although another f_{B} locates at 2.01 GHz, it is not visible in the transmission characteristic but the return loss characteristic.

The frequency response near f_{B} measured at some temperature is stored as a reference, and variation of f_{B} is estimated by taking the correlation of the measured frequency response with the reference.

Measured f_{B} showed linear dependence with that of the Cu plate and no hysteresis was observed.

Figure 4 shows deviation from the linearity. For the evaluation, the temperature coefficient of f_{B} was set at -101 ppm/$^{\circ}$C. The deviation is less than 1°C. This result indicates that this technique can be used for monitoring chip temperature of packaged SAW devices during the PD test.

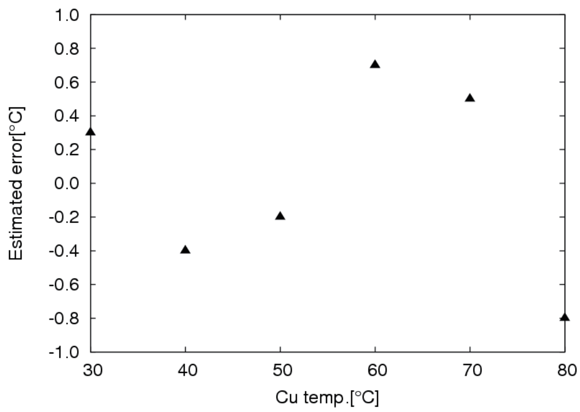


Fig.4 Deviation of the estimated temperature from linearity

4. Conclusion

This paper described construction of an on-wafer measurement system for power durability of SAW/BAW devices, and its applicability was demonstrated. A simple technique for T monitoring was also discussed.

Acknowledgements

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