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Three-level inverter system based on multiplex transmission using surface acoustic wave filters

SAW フィルタを用いた多重化通信による 3 レベルインバータシステムの検証

Keita Kubo[1†], Nanae Kanai[1], Fumiya Kobayashi[1],
Shigeyoshi Goka[1], Keiji Wada[1], and Shoji Kakio[2]
(1Grad. School of Sci. and Eng., Tokyo Metropolitan Univ.; 2Univ. of Yamanashi)
久保 慶太[1†], 金井 七重[1], 小林 史弥[1], 五箇 繁善[1], 和田 圭二[1], 垣尾 省司[2]
([1]首都大・理工, [2]山梨大院・医工)

1. Introduction

Power inverter circuits are used in a wide variety of applications such as domestic appliances, electric cars, trains, and power transmission systems. Next-generation signal transmission systems for inverter circuits need to satisfy the requirements of having simple signal wiring, high dielectric withstanding voltages and high heat resistances[1)]. To address these requirements, we have developed a multiplex transmission system with surface acoustic wave (SAW) filters[2)] and demonstrated half-bridge inverter circuits working with 4-channel SAW filters. Although this system worked well, there was a noticeable transmission delay time variance for each SAW filter because of differences in individual propagation path lengths. Here, we fabricated optimized SAW to reduce the SAW propagation delay time in the proposed system. In this paper, we report the fabrication and characteristics of these 4-channel SAW filters and apply the filters in a single-phase three-level inverter.

2. Configuration of multiplexed transmission system for three-level inverter

Fig.1 shows a schematic of a multiplex transmission system, based on SAW filters, for power inverter systems. In the transmitter, gate control signals are generated by a field-programmable gate array (FPGA), and the RF center frequency of the SAW filters is synthesized by a direct digital synthesizer (DDS) as a frequency modulator of the gate control signals. The center frequency is defined as the frequency at which there is minimum insertion loss of the SAW filters. The generated RF signals are multiplexed by a combiner. The multiplexed RF signal is then transmitted through a single coaxial cable. At a receiver, SAW filters separate each center frequency from the multiplexed RF signals, and the separated signals are demodulated by detector circuits. The demodulated signals are almost the same as the gate control signals that are generated by the FPGA. These signals are amplified by gate driver circuits to control metal-oxide-semiconductor field-effect transistors (MOSFETs), as switching devices for the inverter

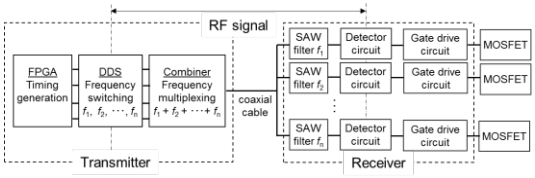

Fig.1 Structure of multiplex transmission system.

Table Ⅰ Specifications of SAW filters.

SAW	Wavelength λ (μm)	Center frequency f_0 (MHz)
No.1	20.0	195
No.2	12.8	308
No.3	9.2	428
No.4	6.0	665

circuits. Here, the number of SAW filters is the same as the number of MOSFETs. In our system, we aimed to achieve a target delay time of less than 2.5 μs, which is 5% of the period of a 20-kHz signal, indicating that the switching operation will be outside of the audible range. The delay time was determined as the time until the gate driver detected a change in the digital status from the change of the FPGA digital output.

3. Design of SAW filters for the multiplexed transmission system

Because a single-phase three-level inverter needs four gate control signals, we used SAW filters having four different center frequencies. The center frequency of the SAW filters were set between 195 and 665 MHz. **Table Ⅰ** shows the SAW filter specifications. We fabricated transversal SAW filters on a 128°Y-X $LiNbO_3$ substrate. The filters featured a voltage endurance between their input and output. Because the assumed voltage endurance was 600 V and the propagation path length was 0.2 mm, the delay times caused by the propagation path were uniform (around 50.3 ns). The fabricated SAW filters had an Al thickness of 1200 Å. **Fig.2** shows the measured insertion losses of the SAW filters. When the frequency was 665 MHz, the suppression ratio

between filters No.1 and No.4 was 7 dB, which remains too high for practical application of our system. The insertion losses arise by signal degradation from electromagnetic waves radiated. **Table Ⅱ** shows the delay time, which is a summation of the rise and fall time of the SAW filters. The rise and fall time was defined as the point when the output reached 63% of its steady-state value. The delay time difference of these SAW filters was less than 321 ns. This is smaller than the previously reported SAW filter delay time difference of 818 ns. Thus, we successfully decreased the delay time difference of our SAW filters by introducing uniform propagation path lengths. When the propagation path lengths are equal, the delay time of the main response will decrease with frequency increases. However, the fall time of filter No.3 was longer than that of No.2, because the TTE of No.3 exceeded its threshold.

4. Results of the three-level inverter using SAW filters

Three-level inverter systems can be used to decrease the size and cost of LC filters in inverter circuits, because the output voltage waveform of a three-level inverter is closer to a sinusoidal waveform than that of a half-bridge inverter. The switching energy loss is also reduced by around 50% because the variation width of the output voltage is halved. Thus, three-level inverters can effectively reduce the size and increase efficiency of these components. **Fig.3** shows the circuit structure of our single-phase three-level inverter system. Here, the dead time was 3 μs and the inverter frequency was 10 kHz. **Fig.4** shows an output voltage waveform of our three-level inverter at 10 kHz. These results confirmed that the output voltages varied in three steps. In the figure, the output voltage is shifted to the positive side. This is because the two electric capacitors, with a nominal value of 2200 μF, showed differences in their capacitance values of about 10%. **Table Ⅲ** shows the delay time of this system. The total delay time was lowered to a maximum of 1.5 μs, which met our delay time requirements. However, the input of the gate driver circuits decreased with an increase in the center frequency, leading to a longer rise time of No.4 than that of other filters.

5. Conclusion

We fabricated an optimized 4-channel SAW filter for a three-level inverter system and measured its characteristics. The measured delay time difference was suppressed to 321 ns or less. This value is less than half that previously reported. We also demonstrated a single-phase three-level inverter based on the fabricated 4-channel SAW filters. The delay time of the inverter system was below our target delay time of 1.5 μs. These results indicate that our system can control switching devices and shows promise for applications in a multi-level inverter system.

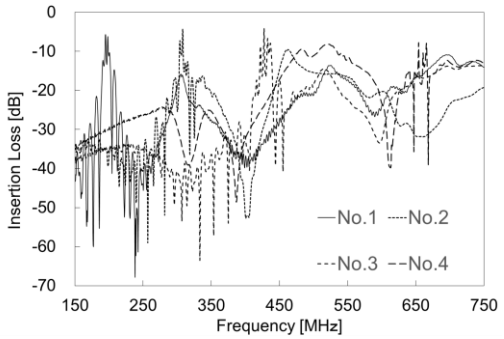

Fig.2 Insertion losses of the SAW filters for the three-level inverter.

Table Ⅱ Delay times of SAW filters.

SAW	Delay times of SAW filters (ns)		
	Rise	Fall	Total (Rise + Fall)
No. 1	372	389	761
No. 2	320	341	661
No. 3	286	391	690
No. 4	168	272	440

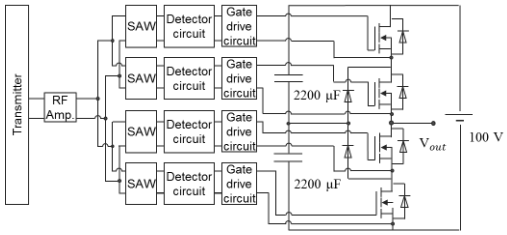

Fig.3 Circuit schematic of the three-level inverter system.

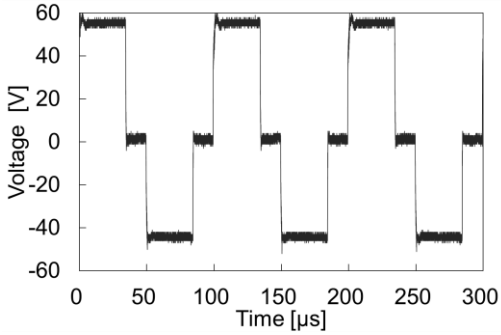

Fig.4 Output voltage waveform of the single-phase three-level inverter at 10 kHz.

Table Ⅲ Delay times of multiplex transmission system

SAW	Delay times of gate signal (μs)			
	Rise	Fall	Total (Rise + Fall)	Target value
No. 1	0.60	0.63	1.23	2.5
No. 2	0.58	0.81	1.39	
No. 3	0.49	0.68	1.17	
No. 4	0.99	0.42	1.41	

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